UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/728,132	12/04/2003	Peter J. Hopper	100-23700 (P05749)	8876

33402 7590 02/28/2006

LAW OFFICES OF MARK C. PICKERING
P.O. BOX 300
PETALUMA, CA 94953

EXAMINER	
NHU, DAVID	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 02/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/728,132	HOPPER ET AL.	
	Examiner	Art Unit	
	David Nhu	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) *16-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15, 21-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

FINAL

DETAILED ACTIONS

Election/Restrictions

1. Applicant's election of Group I (Claims 1-15, 21-24)without traverse is acknowledge.

Claims 1-15, 21-24 are remained for examination. Accordingly, claims 16-20 are canceled/withdra from consideration as being directed to a non-elected invention.

See 37 CFR 1.142(b) and MPEP § 821.03.

Claims Objection

2. Claims 2, 7, 9, 14, **"the** top surface of fourth region" lack a clear antecedent basis.

Claim 21, "**the** top of the fourth region; **the** sidewall of the trench" lack a clear antecedent basis.

Claim 23, " wherein the second and fourth regions include regions with substantially equal dopant concentrations" are not supported/ described in the specifications.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

4. Claims 1-15, 21-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamauchi et al (6,836,001 B2).

Regarding claim 1, Yamauchi, (see figures 2, 15, 16A-16H, 20A-20G, col. 13, lines 1-67. col. 14, lines 1-67, col. 15, 16, lines 1-67, col. 19, lines 30-67, col. 20, lines 1-47), teaches a

transistor comprising: a first region 1 of a first conductivity n-type; a second region 3 of a second conductivity p-type that lies over the first region; a third region 4 of the first conductivity n-type that contacts the second region, the third region being spaced apart from the first region; and a fourth region 5 of the second conductivity p-type that contacts the third region, the fourth region being spaced apart from the second region (see figure 2, col. 6, lines 19-48).

Regarding claim 21, Yamauchi, (see figure 2, col. 6, lines 19-48, 15, 16A-16H, 20A-20G, col. 13, lines 1-67. col. 14, lines 1-67, col. 15, 16, lines 1-67, col. 19, lines 30-67, col. 20, lines 1-47), teaches a transistor comprising: a first region 1 of a first conductivity n-type; a second region 3 of a second conductivity p-type that lies over the first region; a third region 4 of the first conductivity type that contact the second region; a fourth region 5 of the second conductivity type that contacts the third region; a trench 6, 2 having a sidewall 2a that extends from a top surface of the fourth region through the fourth region, the third region, and partially into the second region; a layer of insulation material 7 that contact all the sidewall of the trench 6; and a conductive gate region 8 that contacts the layer of insulation material and fills the trench (see figure 2).

Regarding claim 2, Yamauchi, (see figure 15), also teaches a trench 50, 53 extends from a top surface of fourth region through fourth region, the third region, and partially into second region ; a layer of insulation material 54 that contacts the trench; and a conductive gate region 47 that contacts the layer of insulation material and fills the trench.

Regarding claims 3, 24, Yamauchi teaches the conductive gate region is a region of doped polysilicon 47 (see figures 14, 16 H).

Regarding claim 4, Yamauchi teaches the first, second, third, and fourth regions have a crystallographic orientation (see figures 2, 9, 11, 13).

Regarding claims 5, 6, Yamauchi teaches a plug 6 that is formed through the first region to contact the second region (see figures 2, 9); wherein the plug is metallic.

Regarding claims 7, 14, Yamauchi also teaches a layer of isolation material that contacts a top surface of the fourth region, the layer of insulation material 54, and the conductive gate region 47; a gate contact formed through the layer of isolation material to make an electrical connection with the conductive gate region; and a drain 52 contact formed through the layer of isolation material to make an electrical connection with the fourth region (see figure 15).

Regarding claims 8, 22, Yamauchi teaches an insulating layer that contacts the first and second regions (see figure 2).

Regarding claim 9, Yamauchi teaches a plurality of trenches 6 that extend from a top surface of fourth region through the fourth region, the third region, and partially into second region; a plurality of insulation layers that contact the plurality of trenches such that each trench has an insulation layer; and a plurality of conductive gate regions that contact the plurality of insulation layer and fill up the trenches (see figures 2, 9, 11, 13).

Regarding claim 10, Yamauchi teaches the plurality of conductive gate regions 8 are regions of doped polysilicon (see figures 2, 9).

Regarding claim 11, Yamauchi teaches the first, second, third, and fourth regions have a crystallographic orientation (see figures 2, 9, 11, 13).

Regarding claims 12, 13, Yamauchi also teaches a plug that is formed through the first region to contact the second region (see figures 20A-20D), wherein the plug is metallic.

Regarding claim 15, Yamauchi teaches an insulating layer that contacts the first and second regions (see figures 11, 13).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Blanchard'722, Blanchard'785, Ohno'753, Andoh'301, Williams'463 are cited as of interest.

6. A shortened statutory period for response to this action is set to expired 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned(see 710.02 (b)).

7. Any inquiry concerning this communication on earlier communications from the examiner should be directed to David Nhu (571)272-1792. The examiner can normally be reached on Monday-Friday from 7:30 AM to 5:00 PM. The examiner's supervisor, David Nelms can be reached on (571)272-1787.

The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Information regarding the status of an application may be obtained from the patent application information retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David Nhu

September 22, 2005